```
=> d his

     (FILE 'USPAT' ENTERED AT 10:53:50 ON 07 DEC 1998)
L1         26804 S MEMORY(2W)ADDRESS
L2          4274 S FIRST(W)LATCH
L3          4780 S SECOND(W)LATCH
L4           421 S L1 AND L2 AND L3
L5         17845 S (OUTPUT(2W)ENABLE) OR OE
L6          5567 S (ROW(W)ADDRESS(W)STROBE) OR RAS
L7            21 S L4 AND L5 AND L6

=> d l7 1-
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1. 5,831,931, Nov. 3, 1998, Address strobe recognition in a memory device; Troy Manning, 365/233.5, 230.08, 239 [IMAGE AVAILABLE]

2. 5,813,023, Sep. 22, 1998, Method and apparatus for multiple latency synchronous dynamic random access memory; Loren L. McLaury, 711/105; 365/189.08, 194, 233; 711/167 [IMAGE AVAILABLE]

3. 5,793,688, Aug. 11, 1998, Method for multiple latency synchronous dynamic random access memory; Loren L. McLaury, 365/203, 233; 711/105 [IMAGE AVAILABLE]

4. 5,784,599, Jul. 21, 1998, Method and apparatus for establishing host bus clock frequency and processor core clock ratios in a multi-processor computer system; Bassam N. Elkhoury, 395/556 [IMAGE AVAILABLE]

5. 5,768,624, Jun. 16, 1998, Method and apparatus for employing ping-pong buffering with one level deep buffers for fast DRAM access; Subir K. Ghosh, 395/873; 711/157 [IMAGE AVAILABLE]

6. 5,734,914, Mar. 31, 1998, Computer system capable of shifting voltage level of data signal between processor and system memory; Nobutaka Nakamura, et al., 395/750.01 [IMAGE AVAILABLE]

7. 5,734,617, Mar. 31, 1998, Shared pull-up and selection circuitry for programmable cells such as antifuse cells; Hua Zheng, 365/225.7, 100 [IMAGE AVAILABLE]

8. 5,655,105, Aug. 5, 1997, Method and apparatus for multiple latency synchronous pipelined dynamic random access memory; Loren L. McLaury, 711/169; 365/194; 711/105 [IMAGE AVAILABLE]

9. 5,652,723, Jul. 29, 1997, Semiconductor memory device; Katsumi Dosaka, et al., 365/189.01, 189.03, 230.03 [IMAGE AVAILABLE]

10. 5,640,364, Jun. 17, 1997, Self-enabling pulse trapping circuit; Todd Merritt, et al., 365/233.5, 206, 230.08 [IMAGE AVAILABLE]

11. 5,636,370, Jun. 3, 1997, System and method for interfacing risc busses to peripheral circuits using another template of busses in a data

communication adapter; Patrick Sicsic, et al., 395/500 [IMAGE AVAILABLE]

12. 5,603,009, Feb. 11, 1997, Semiconductor memory device including a data transfer circuit for transferring data between a DRAM and an SRAM; Yasuhiro Konishi, et al., 711/165; 365/189.05, 230.03; 711/104 [IMAGE AVAILABLE]

13. 5,590,287, Dec. 31, 1996, Configurable interface for routing data between mismatched devices; Charles P. Zeller, et al., 395/307; 364/DIG.1, DIG.2; 395/500 [IMAGE AVAILABLE]

14. 5,539,696, Jul. 23, 1996, Method and apparatus for writing data in a synchronous memory having column independent sections and a method and apparatus for performing write mask operations; Vipul C. Patel, 365/189.01, 189.05, 230.03, 233 [IMAGE AVAILABLE]

15. 5,539,430, Jul. 23, 1996, Pipelined read write operations in a high speed frame buffer system; Curtis Priem, et al., 345/507, 509, 515 [IMAGE AVAILABLE]

16. 5,530,955, Jun. 25, 1996, Page memory device capable of short cycle access of different pages by a plurality of data processors; Katsuyuki Kaneko, 711/104; 364/228.1, 249, 254.3, DIG.1; 365/189.05, 230.02, 238.5; 711/105, 147 [IMAGE AVAILABLE]

17. 5,450,364, Sep. 12, 1995, Method and apparatus for production testing of self-refresh operations and a particular application to synchronous memory devices; Michael C. Stephens, Jr., et al., 365/222, 201, 230.08 [IMAGE AVAILABLE]

18. 5,386,385, Jan. 31, 1995, Method and apparatus for preventing invalid operating modes and an application to synchronous memory devices; Michael C. Stephens, Jr., 365/189.05, 189.01, 195 [IMAGE AVAILABLE]

19. 5,305,278, Apr. 19, 1994, Semiconductor memory device having block write function; Kazunari Inoue, 365/230.03, 189.01, 189.05 [IMAGE AVAILABLE]

20. 5,289,584, Feb. 22, 1994, Memory system with FIFO data input; Gary W. Thome, et al., 711/109; 364/926.3, 939.1, 964.33, 966.3, DIG.2; 365/219, 230.04; 711/157 [IMAGE AVAILABLE]

21. 5,287,327, Feb. 15, 1994, Synchronous dynamic random access memory; Atsushi Takasugi, 365/230.02, 189.05, 230.08, 233.5 [IMAGE AVAILABLE]